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Reduction of Common-Mode Voltages for Five-Level Active NPC Inverters by Space Vector Modulation Technique

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***Abstract*--In this paper, a novel space vector pulse width modulation (SVPWM) scheme for reducing the common-mode voltage (CMV) in the three-phase five-level active neutral-point clamped (5L-ANPC) inverter is proposed, where only the 55 selected voltage vectors among the entire 125 ones that produce low values of the CMV are utilized. This PWM scheme can significantly reduce the CMV without the increase of switching losses and total harmonic distortion (THD) of the output voltages. With the 55 selected voltage vectors, the inverter can still operate up to the maximum modulation index (MI). In addition, the capacitor voltages are controlled by redundant switches of the 5L-ANPC inverters. It has been shown that the peak value of the CMV is decreased to one twelfth of the DC-link voltage from the simulation and experimental results.**

***Index Terms*—Active neutral point clamped inverter, common-mode voltage, multilevel inverter, space vector pulse width modulation.**

I. Introduction

The common-mode voltage (CMV) produced in the PWM inverters is one of the causes of leakage currents and voltage stresses in the AC machine drive systems, which affects the lifetime of the electric machine [1]. To reduce or eliminate the effects of the CMV on the electric machines, a lot of research results have been introduced [2]–[21].

For the three-level PWM inverters, the CMV can be cancelled if the medium and zero voltage vectors are adopted appropriately with the large and small vectors excluded [9]–[11]. However, such a restrictive utilization of voltage vectors is responsible for the increase of switching losses and total harmonic distortion (THD) of output voltage as well as a decreased linear output range of the inverter. In addition, the neutral-point voltage (NPV) cannot be controlled appropriately since several redundant voltage vectors which cause a high CMV should not be involved [9]. Another SVPWM for reducing the CMV of three-level neutral-point clamped (NPC) inverters has been proposed [13], where only 19 voltage vectors generating a low CMV among the whole 27 ones are utilized. This method can reduce the CMV to one sixth of the DC-link voltage, V_{dc}. However, this PWM scheme cannot control the NPV by itself.

For five-level NPC inverters, a PWM scheme which can reduce the CMV up to V_{dc}/12, by utilizing only 55 voltage vectors producing low CMV values, was introduced [15]. In this research, however, the DC-link capacitor voltage balance has not been investigated, where the four controllable DC sources are required. For three-phase five-level cascaded H-bridge inverters with six isolated DC sources, the CMV value can be decreased to V_{dc}/12 [16]. In these schemes, the CMV can be reduced successfully without the DC capacitor voltage control. Therefore, it is difficult to apply to five-level active neutral-point clamped (5L-ANPC) inverters.

The three-phase 5L-ANPC is an appropriate candidate for high-power motor drive applications since it has advantages such as high efficiency, simple structure and control, and improved output performance [22], [23]. One PWM method for the CMV reduction was introduced in [18], of which aims are to balance the DC-link capacitor voltages, to control the flying capacitor voltage, to minimize the switching frequency of higher-voltage-rated devices, and to reduce the CMV. In [18], the voltage offset component is utilized to control the DC-link capacitor voltage. The flying capacitor voltage is controlled by values of current and flying-capacitor voltage deviation. However, the peak of CMV is still high, which is about V_{dc}/4, which can cause some serious effect of CMV. Therefore, this paper provides the SVPWM method to reduce the CMV to V_{dc}/12.

This paper proposes a novel SVPWM technique for the three-phase 5L-ANPC inverters, which can alleviate the CMV to V_{dc}/12, where only the 55 voltage vectors are employed. In addition, the flying-capacitor and DC-link voltages are controlled by selecting the appropriate switching states. Furthermore, the proposed SVPWM can still keep most of advantages of 5L-ANPC inverters, where the switching frequency of high-voltage-rated switches is equal to the fundamental one. The effectiveness of the proposed SVPWM scheme is verified by the simulation and experimental results.

II. Five-Level ANPC Inverters

A. Configuration

The structure of a single-phase leg of 5L-ANPC inverters is shown in Fig. 1(a), which is composed of eight switches, one flying capacitor, and two DC-link capacitors [24]. The

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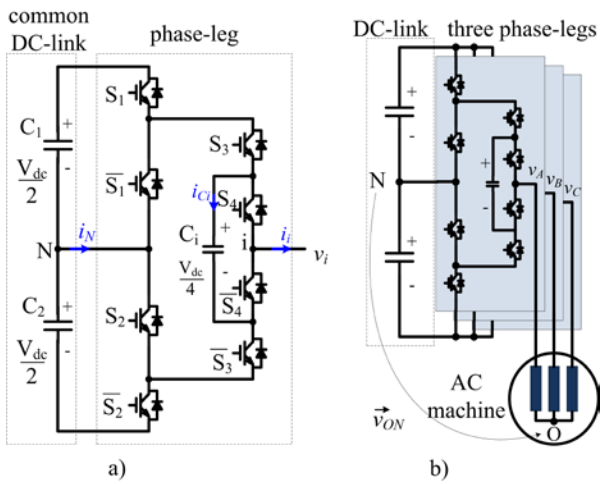

Fig. 1. Structure of 5L-ANPC inverters. (a) Phase leg and common DC-link. (b) Three-phase inverter for AC machine drives.

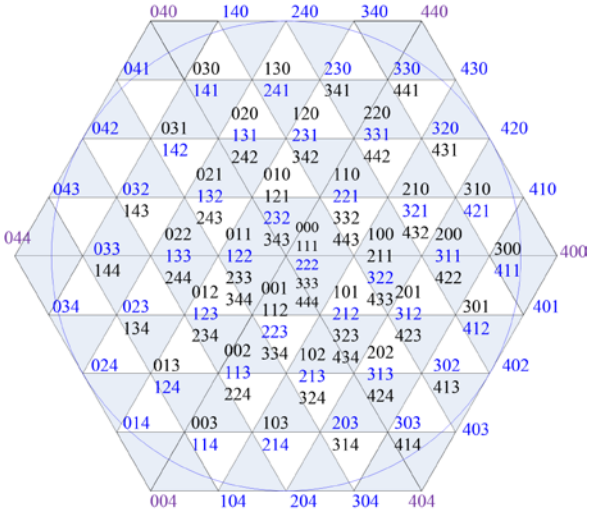

Fig. 2. Voltage vectors of 5L-ANPC inverter.

TABLE I. SWITCHING STATE OF 5L-ANPC INVERTERS

Switching states	v_{jN}	Switching function (S_j)	S_1	S_2	S_3	S_4	i_{Cj}	i_N
V_0	$-V_{dc}/2$	0	0	0	0	0	0	0
V_1	$-V_{dc}/4$	1	0	0	0	1	$-i_j$	0
V_2	$-V_{dc}/4$	1	0	0	1	0	i_j	i_j
V_3	0	2	0	0	1	1	0	i_j
V_4	0	2	1	1	0	0	0	i_j
V_5	$V_{dc}/4$	3	1	1	0	1	$-i_j$	i_j
V_6	$V_{dc}/4$	3	1	1	1	0	i_j	0
V_7	$V_{dc}/2$	4	1	1	1	1	0	0

voltage ratings of switches, S_1, S_2, and DC-link capacitors are a half of DC-link voltage, whereas the rated values of switches, S_3, S_4, and flying capacitors are $V_{dc}/4$. It is known that the switching frequency of S_1 and S_2 can be kept at the fundamental one, which is an important benefit of this inverter topology. In each leg of 5L-ANPC inverters, there are four complementary switch pairs such as S_1 and $\overline{S}_1$, S_2 and $\overline{S}_2$, S_3 and $\overline{S}_3$, S_4 and $\overline{S}_4$.

B. Operating Principle

The switching states of the 5L-ANPC inverter are listed in Table I. It is seen that the S_1 and S_2 can be controlled by the same gating signal. The 5L-ANPC inverter has eight distinctive switching states, which produce the five different voltage levels. So, there are several redundant switching states which generate the same output voltage level but differently affect the flying capacitor voltage and NPV. For example, the voltage level of $V_{dc}/4$ can be generated by either V_5 or V_6. Therefore, the capacitor voltages of the 5L-ANPC inverter can be controlled by selecting the redundant switching states appropriately according to the capacitor voltages and phase currents.

For the SVPWM of the 5L-ANPC inverter, there are 125 voltage vectors as shown in Fig. 2, among which the three nearest voltage vectors are combined to produce the reference voltage [20]. In this research, each group of the three nearest voltage vectors is selected for minimizing the deviation of the NPV and the THD, where the DC-link capacitor voltages are controlled by the redundant voltage vectors.

C. CMV of the 5L-ANPC inverter

Fig. 1(b) shows the three-phase 5L-ANPC inverter for AC machine drives. At first, the CMV of the machine drive system, v_{ON}, is defined as the voltage difference between two neutral points of the machine and the DC bus of the inverter, which is expressed as

$$v_{ON} = (v_{AN} + v_{BN} + v_{CN})/3 \quad (1)$$

where v_{AN}, v_{BN}, and v_{CN} are the pole voltages of the inverter [13].

III. EFFECTS OF REDUNDANT SWITCHING STATES ON THE CAPACITOR VOLTAGES

In this section, the effects of redundant switching states on the DC-link and flying capacitor voltages are investigated.

The two redundant switching states of V_1 and V_2 producing the same voltage level of $-V_{dc}/4$ affect the DC-link and flying capacitor voltages differently. For the positive phase current, for example, the V_1 discharges the flying capacitor and does not affect the NPV, but the V_2 charges the flying capacitor and decreases the NPV, which are shown in Fig. 3(a) and (b), respectively. That is, the flying capacitor voltage is controlled priorly. Next, if the flying capacitor voltage is in the acceptable range, the switching state of V_1 and V_2 is utilized to control the DC-link capacitor voltages. For the negative phase current, their effects on the DC-link and flying capacitor voltages are reversed.

Meanwhile, the switching states of V_5 and V_6 producing

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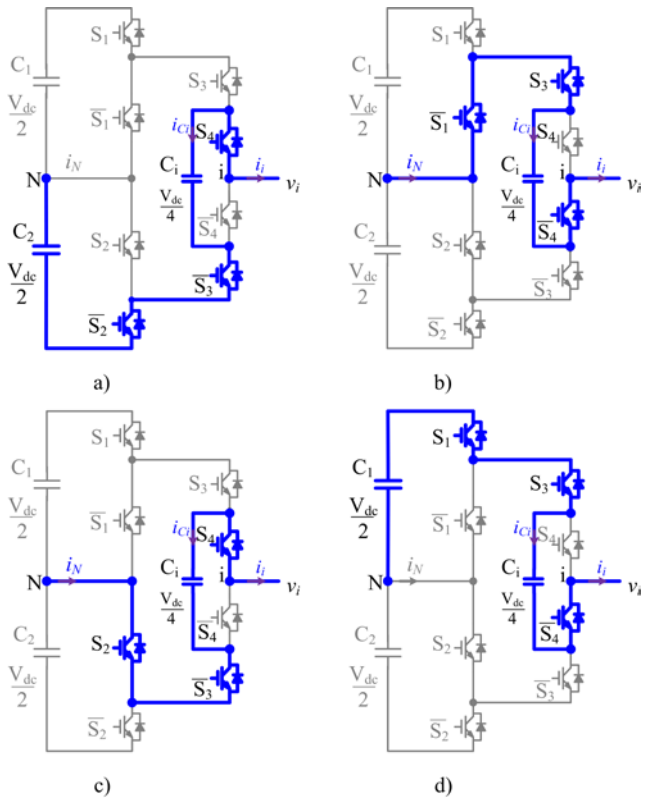

Fig. 3. Effects of redundant switching states on the capacitor voltages. (a) V_1. (b) V_2. (c) V_5. (d) V_6.

the same voltage level of $V_{dc}/4$ affect the DC-link and flying capacitor voltages differently, which are shown in Fig. 3(c) and (d), respectively. For the positive phase current, the V_5 decreases both the NPV and flying capacitor voltage, whereas the V_6 increases the flying capacitor voltage but does not affect the NPV.

IV. Proposed SVPWM Technique

A. Selecting Voltage Vectors for Low CMVs

The CMVs of 125 voltage vectors of the 5L-ANPC vary from $-V_{dc}/2$ to $V_{dc}/2$ with a step change of $V_{dc}/12$. The CMV generated by each voltage vector can be calculated as [15]

$$v_{ON} = \frac{V_{dc}}{12}(S_A + S_B + S_C - 6) \tag{2}$$

where S_A, S_B, and S_C are the switching functions of each leg of the inverter, respectively, where their values are 0 to 4 as shown in Fig. 2.

Among all 125 voltage vectors of the regular SVPWM, the proposed scheme uses 55 ones, which make the CMVs vary from $-V_{dc}/12$ to $V_{dc}/12$. It is noted that the six voltage vectors at the vertices of hexagon with a high CMV generation, $\pm V_{dc}/6$, are excluded, where the inverter can still operate up to the maximum modulation index (MI). The result of this selection strategy called as *case-1* is shown in Fig. 4, where the 55 voltage vectors can cover the full range of MI, that is, the inscribed circle of hexagon.

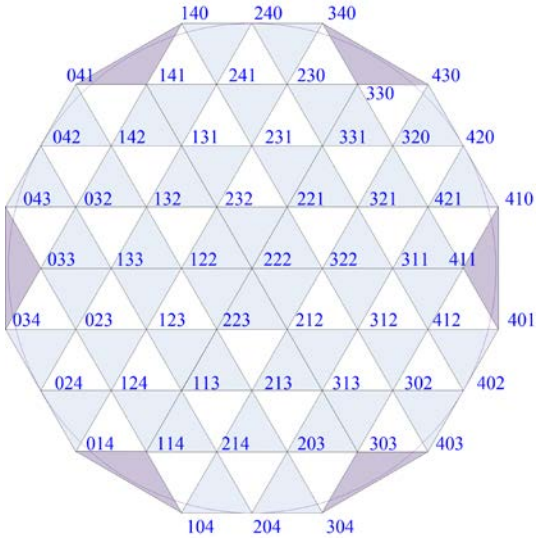

Fig. 4. Selected voltage vectors for CMV reduction of 5L-ANPC inverter (case-1).

TABLE II. Selected Switching States for Flying Capacitor Voltages Control

Flying capacitor voltage control signal	DC-link capacitor voltage control signal	Switching states
$Sig\_Fly_j \geq 0$	$Sig\_DC_j \geq 0$	V_0, $\boldsymbol{V_1}$, V_3, V_4, $\boldsymbol{V_5}$, V_7
$Sig\_Fly_j < 0$	$Sig\_DC_j < 0$	V_0, $\boldsymbol{V_2}$, V_3, V_4, $\boldsymbol{V_6}$, V_7

B. Control of Flying Capacitor Voltages

All flying capacitor voltages should be kept at $V_{dc}/4$, which can be easily achieved by selecting the redundant switching states appropriately. The deviation of the flying-capacitor voltage is defined as

$$\Delta v_{f\_j} = v_{f\_j} - V_{dc}/4 \qquad (j = a,b,c) \tag{3}$$

where v_{f_j} is the flying-capacitor voltage of phase $\boldsymbol{j}$.

For selecting the switching state, the control signal parameters of the flying capacitor voltage, Sig_Fly_j, and DC-link capacitor voltage, Sig_DC_j, are introduced. The Sig_Fly_j is defined as:

$$Sig\_Fly_j = \Delta v_{f\_j} i_j \qquad (j = a,b,c) \tag{4}$$

where i_j is the measured current of phase $\boldsymbol{j}$.

The switching states to be selected for controlling the flying-capacitor voltage are listed in Table II. If the Sig_Fly_j is positive, one group of the switching states of V_0, V_1, V_3, V_4, V_5, and V_7 is selected. If it is negative, the other group is selected. The parameter of Sig_DC_j in Table II will be explained later.

For example, the Sig_Fly_j is positive, which means both Δv_{f_j} and i_j are positive or negative together, the switching state of V_1 is chosen for the voltage level of $-V_{dc}/4$. This switching state discharges the flying capacitor when Δv_{f_j} and

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i_j are positive as shown in Fig. 3(a), and vice versa.

C. Control of the NPV

The DC-link capacitor voltages of 5L-ANPC inverters can be self-balanced in a fundamental cycle when the three-phase load is balanced [23]. For the motor drive applications, the three-phase load is normally balanced, thus the DC-link capacitor voltages can be balanced.

In the case of the unbalanced DC-link capacitor voltages, the voltage vectors which can regulate the NPV are selected by priority. Also, it is desirable that the CMV of the inverter is lowered as far as possible, where the peak value of the CMV is $V_{dc}/6$.

The deviation of the NPV is defined as

$$\Delta v_n = \frac{v_{C2} - v_{C1}}{2} \tag{5}$$

where v_{C1} and v_{C2} are the voltages of the upper and lower DC-link capacitors, respectively. The *case-1* SVPWM is modified to control the NPV. The fifteen voltage vectors which produce the value of CMVs at $V_{dc}/6$ are selected to replace the voltage vectors by the negative CMVs of $-V_{dc}/12$ as shown in Fig. 5(a). For example, the voltage vector of {320} is replaced by the voltage vector of {431} for the purpose of NPV control. This group of voltage vectors called as *case-2* is utilized to increase the NPV. On the other hand, the fifteen voltage vectors which generate the CMV value of $-V_{dc}/6$ are chosen to replace the ones by the negative CMVs of $V_{dc}/12$ as shown in Fig. 5(b). For instance, the voltage vector of {310} replaces the one of {421}. This group of voltage vectors called as *case-3* is used to decrease the NPV.

D. Improvement for DC-Link Capacitor Voltage Balance

In the case of balanced DC-link capacitor voltages, that is *case-1* SVPWM, the peak value of NPV fluctuation can be reduced by selecting the switching states appropriately. In this case, when the error of the flying-capacitor voltages is low, that is $\left|\Delta v_{f\_j}\right| < \Delta v_{f\_\max}$, the redundant switching states can be used to improve the DC-link capacitor voltage balance. For a switching state selection, the control signal of DC-link capacitor voltages, Sig_DC_j, is defined as

$$Sig\_DC_j = \Delta v_n i_j v_j^* \qquad j = (a,b,c) \tag{6}$$

where Δv_n is the deviation of the NPV, i_j and v_j^* are the current and the reference voltage of phase ***j,*** respectively. The switching states selected according to the polarity of Sig_DC_j, are listed in Table II.

For example, the negative Δv_n, i_j and the positive reference voltage leads to the positive Sig_DC_j. The switching state of V_5 is selected for voltage level of $V_{dc}/4$ at this condition according to Table II. For this switching state, the neutral-point current, i_n, discharges the capacitor C_2 and causes a reduction Δv_n. The signal of Sig_DC_j can keep the DC-link capacitor voltage balancing.

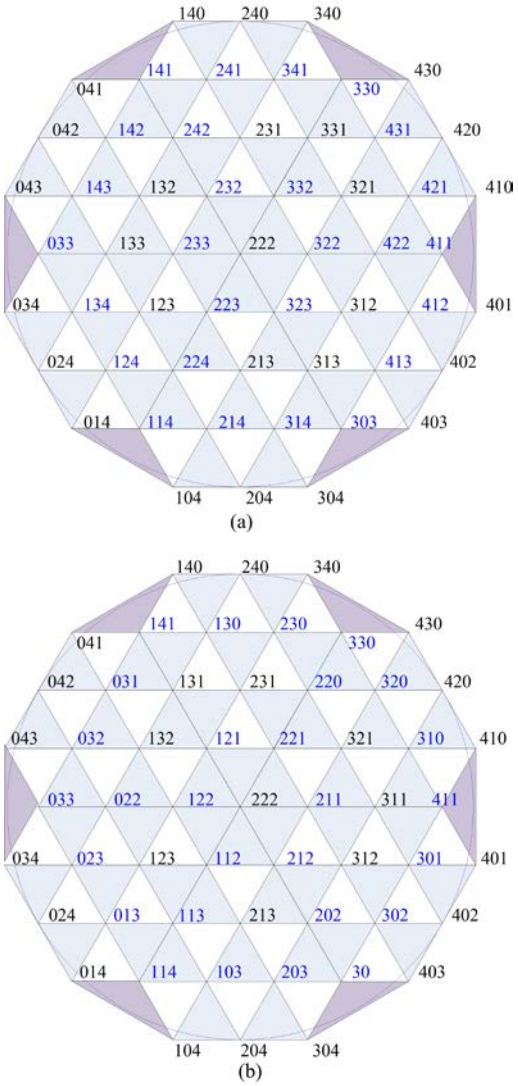

Fig. 5. Voltage vectors with control capability of NPV and low CMV. (a) For increasing NPP (case-2). (b) For decreasing NPP (case-3).

E. Implementation for the Proposed Scheme

Fig. 6 shows the flow chart of the proposed SVPWM scheme. When the reference voltage vector, v_{ref}, is given, the sector and region in the space vector diagram are determined. According to the deviation of the NPV, Δv_n, a relevant case of SVPWM is selected.

When the Δv_n is within the Δv_{n_max}, which is usually 5% of the rated value, *case-1* PWM is chosen. In this case, the CMV is $V_{dc}/12$. If the Δv_n is larger than the Δv_{n_max}, case-2 or case-3 SVPWM method is selected, which can control the NPV depending on the polarity of the Δv_n. For *case-2* and *case-3* SVPWM methods, the CMV can be $V_{dc}/6$ in the transient states while the balancing control of the DC-link capacitor voltage is applied. However, this value of the CMV rarely appears since the DC-link voltage is almost all the time

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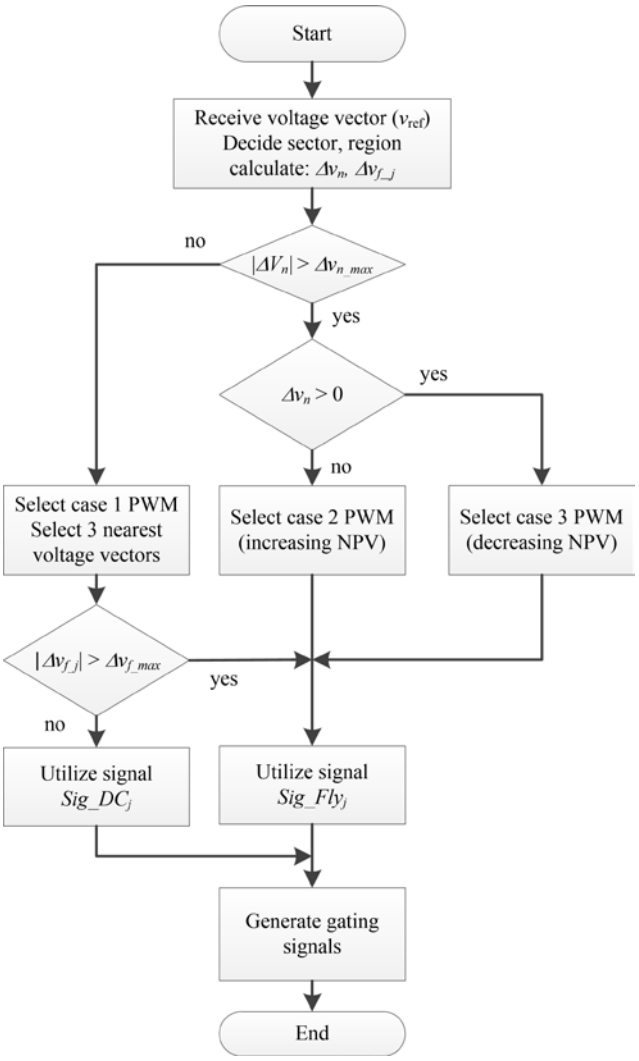

Fig. 6. Flow chart for the proposed algorithm.

balanced well, except initial operation, by the method described in the previous subsection.

For case-2 and case-3 SVPWM methods, the Sig_Fly_j signal is used to control the flying capacitor voltage, which is listed in Table II. For *case-1* SVPWM, the deviation of the flying capacitor voltage is compared with the Δv_{f_max}. From the result of comparison, either Sig_DC_j or Sig_Fly_j is selected as listed in Table II.

V. Simulation Results

The simulation tests of the 5L-ANPC inverter were carried out to verify the effectiveness of the proposed SVPWM scheme using PSIM software. The parameters of the 5L-ANPC inverter are listed in Table III, which feeds a 1,000-kW and 4,160-V induction motor controlled by a constant V/f mode.

Fig. 7 shows the voltage and current waveforms of the

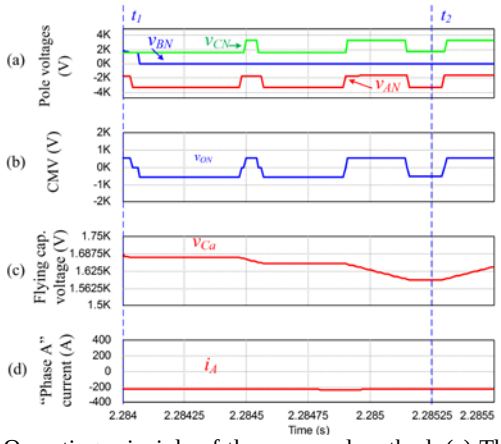

Fig. 7. Operating principle of the proposed method. (a) Three-phase pole voltages. (b) CMV. (c) Phase-A flying-capacitor voltage. (d) Phase-A current.

TABLE III. Simulation Parameters of 5L-ANPC Inverters

Parameters	Values
DC input voltage	6,500 V
DC-link capacitance	2,000 μF
Flying capacitance	1,000 μF
Switching frequency	2,000 Hz
$\Delta v_{n\ max}$	162 V
$\Delta v_{f\ max}$	41 V

5L-ANPC inverter with the proposed SVPWM. Fig. 7(a) shows the three-phase pole voltages with a step change of $V_{dc}/4$ (1,625 V). The CMV defined in (1), which varies among –541.6 V, 0 V, and 541.6 V, is shown in Fig. 7(b). The flying capacitor voltage and load current of the phase-A are shown in Fig. 7(c) and (d), respectively. At $t = t_1$ the flying capacitor voltage is higher than its reference of $V_{dc}/4$ = 1,625 V, and the negative current gives the negative Sig_Fly_a. Therefore, at the phase-A pole voltage of –1,625 V, the V_2 is applied to discharge the flying capacitor, of which voltage is decreased as shown in Fig. 7(c). When the flying capacitor voltage is lower than its reference at $t = t_2$, the Sig_Fly_a becomes positive and the V_1 is applied to charge the flying capacitor if the reference voltage is $-V_{dc}/4$.

Fig. 8 shows the performance of the 5L-ANPC inverter with the conventional PWM method [18] at rated speed of the induction motor. Fig. 8(a) shows the line-to-line voltage, v_{AB}, which has nine voltage levels, of which THD is about 17.02%. The three-phase current waveforms are illustrated in Fig. 8(b), which are sinusoidal. The switching frequency of the S_{A1} and S_{A2} is the same as the fundamental one as shown in Fig. 8(c). The DC-link capacitor voltages for the 5L-ANPC inverter is illustrated in Fig. 8(d). The ripple components of the DC-link capacitor voltages are about 0.8%. The flying-capacitor voltages are controlled at their reference values as shown in Fig. 8(e). The CMV of the 5L-ANPC inverter is shown in Fig. 8(f), where its RMS and peak values

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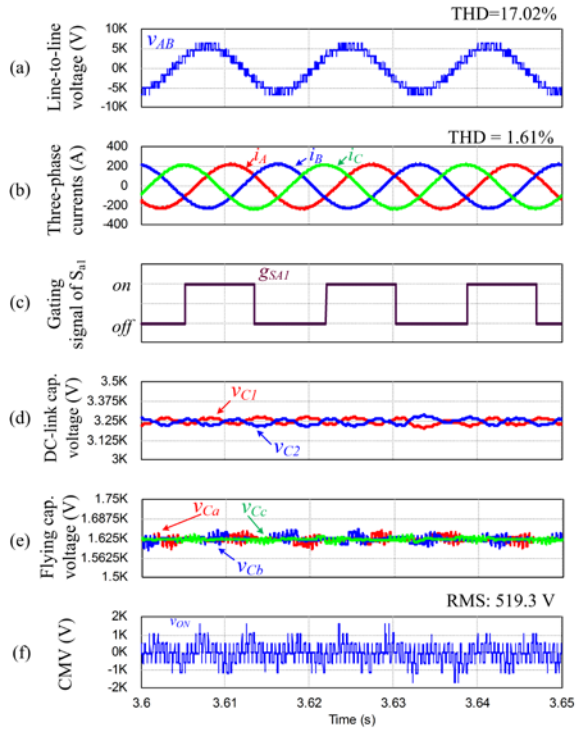

Fig. 8. Operation of the 5L-ANPC inverter with conventional. (a) Line-to-line voltage. (b) Three-phase currents. (c) Gating signal of S_{a1}. (d) DC-link capacitor voltages. (e) Flying capacitor voltages. (f) CMV.

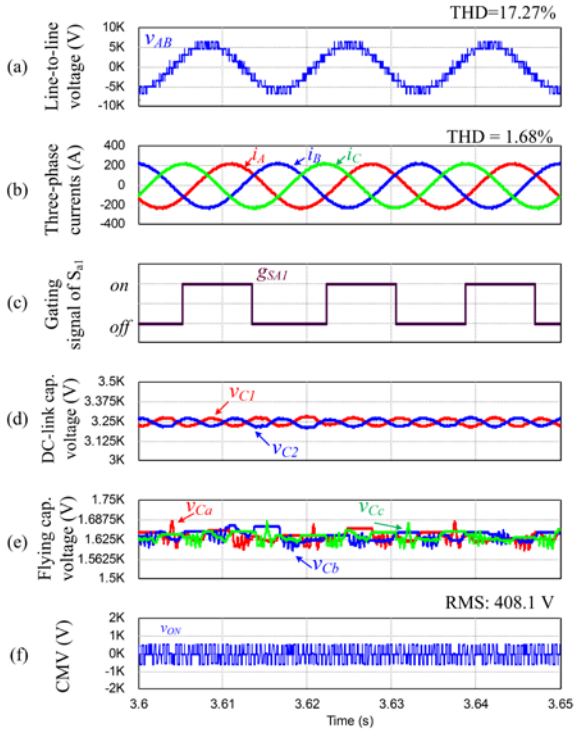

Fig. 9. Operation of the 5L-ANPC inverter with the proposed method. (a) Line-to-line voltage. (b) Three-phase currents. (c) Gating signal of S_{a1}. (d) DC-link capacitor voltages. (e) Flying capacitor voltages. (f) CMV.

are 519.3 V and 1,625 V, respectively.

The operating performance of the 5L-ANPC inverter with the proposed SVPWM is shown in Fig. 9, which is compared with Fig. 8. The THD of the line-to-line voltage in Fig. 9(a) is 17.27%, as good as that of the conventional method. Fig. 9(c) shows the gating signal of the devices S_{A1} operating at fundamental switching frequency, which can keep the inverter switching losses low. Fig. 9(d) shows the DC-link capacitor voltages which are fluctuated slightly larger than that of the conventional one. However, it is still kept within about 1% of the reference value. Fig. 9(e) shows the flying-capacitor voltages, which are well controlled at the reference values. Although some voltage vectors are missing to balance DC-link and flying capacitor voltages, the redundant switching states of the inverter can keep all the capacitor voltages close to their reference values. The CMV in Fig. 9(f) is just 542 V in peak and 408.1 V in RMS value, which is much lower than those of in the conventional PWM.

Fig. 10 shows the balancing capability of the DC-link capacitor voltages. Initially, the capacitor voltages of v_{C1} and v_{C2} are unequal at $t = t_0$, thereafter with the proposed SVPWM they are balanced at $t = t_1$ as shown in Fig. 10(a), where the time to balance is about 100 ms. The flying capacitor voltages are well controlled during this duration as shown in Fig. 10(b). Fig. 10(c) shows the CMV, which

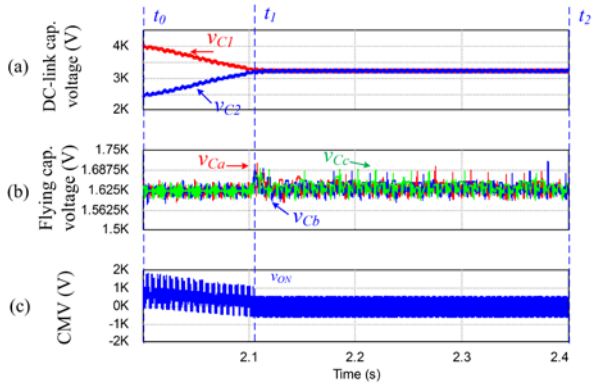

Fig. 10. Balancing control of DC-link capacitor voltages. (a) DC-link capacitor voltages. (b) Flying capacitor voltages. (c) CMV.

reaches the high peak value of $V_{dc}/6$ due to *case-2* SVPWM applied from $t = t_0$ to $t = t_1$. *From* $t = t_1$, *case-1* SVPWM is employed with a low CMV of $V_{dc}/12$.

The inverter performances for the transient conditions are shown in Fig. 11 and Fig. 12. Fig. 11 shows that the change of the rotor speed does not affect the capability of the capacitor voltage control. The motor speed is changed from 900 rpm to 1,780 rpm at $t = 2$ s and back to 900 rpm at $t = 2.4$ s as shown in Fig. 11(a). The inverter voltage corresponding to the motor speed is shown in Fig. 11(b). In this duration, all the capacitor voltages are controlled as their reference values

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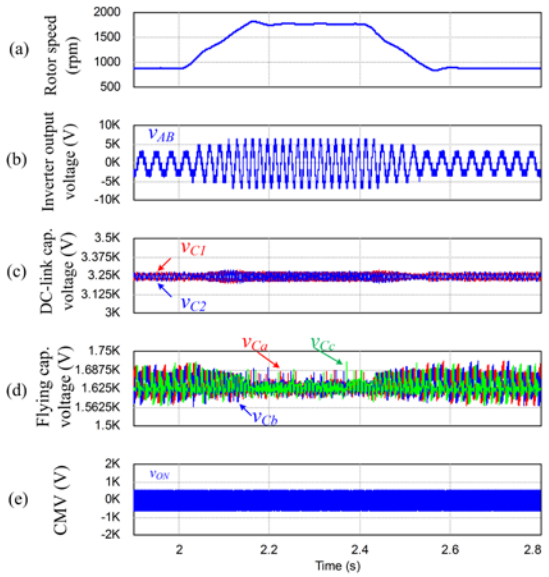

Fig. 11. Performance for speed transients of induction motor drives. (a) Rotor speed. (b) Output voltage. (c) DC-link capacitor voltages. (d) Flying capacitor voltages. (e) CMV.

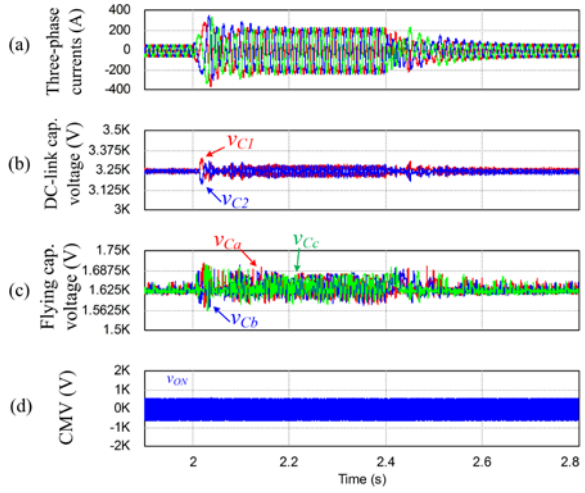

Fig. 12. Performance for torque transients of induction motor drives. (a) Three phase currents. (b) DC-link capacitor voltages. (c) Flying capacitor voltages. (d) CMV.

as shown in Fig. 11(c) and (d), whereas the CMV of the inverter is decreased to $V_{dc}/12$ as shown in Fig. 11(e). On the other hand, Fig. 12 shows the capability of both the DC-link and flying capacitor voltage controls when the load condition is changed from full load to no load at t = 2 s and back to no load at time = 2.4 s. It is seen that the capacitor voltages are well controlled and the CMV is kept as $V_{dc}/12$ in transient states. Due to the increase of the load current, the fluctuation of the capacitor voltages are increased, but still within the allowable range.

Fig. 13 shows the performance of the 5L-ANPC inverter

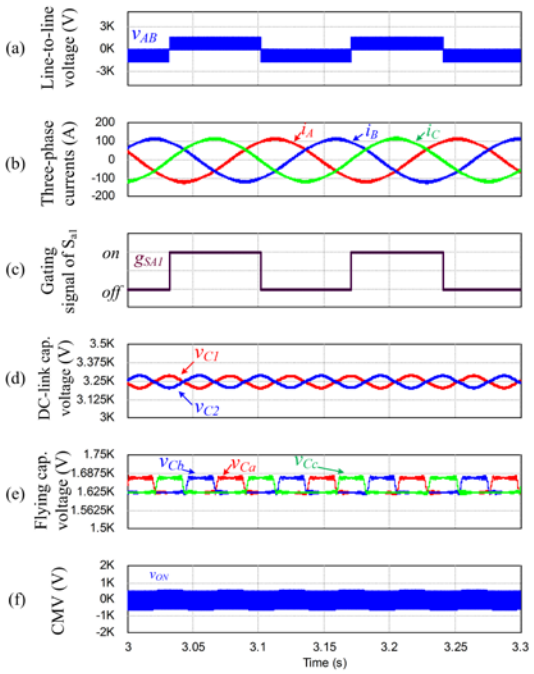

Fig. 13. Operation of the 5L-ANPC inverter at low speed of induction motor. (a) Line-to-line voltage. (b) Three-phase currents. (c) Gating signal of S_{a1}. (d) DC-link capacitor voltages. (e) Flying capacitor voltages. (f) CMV.

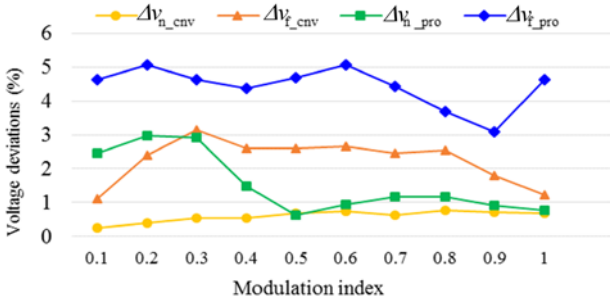

Fig. 14. Comparison of deviations in the capacitor voltages.

for the induction motor operating at low speed (200 rpm) and no load conditions. The output voltage has the three voltage steps as the two-level inverter as shown in Fig. 13(a). The gating signal of the S_{A1} in Fig. 13(c) shows that this device is switched at a fundamental frequency. The DC-link and flying capacitor voltages are controlled at their reference values, which their fluctuations are about 1% and 3.5% as shown in Fig. 13(d) and (e), respectively. Fig. 13(f) shows that the CMV is reduced to $V_{dc}/12$.

Fig. 14 shows the comparison of the capacitor voltage deviation, where the symbols of Δv_{n_Cnv} and Δv_{f_Cnv} represent the deviations of the flying and DC-link capacitor voltages, respectively, of the conventional PWM method. Also, the Δv_{n_Pro} and Δv_{f_Pro} correspond to those of the proposed scheme, respectively. It is noted that in the proposed

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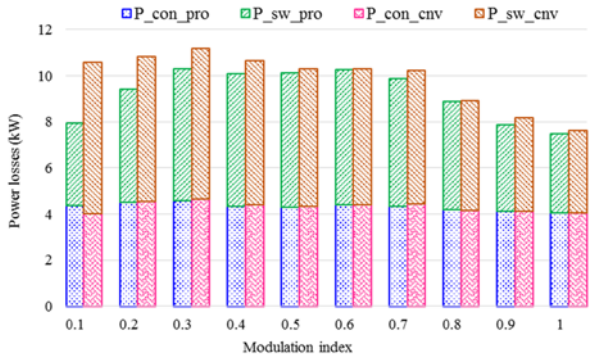

Fig. 15. Power losses of the 5L-ANPC inverter for the proposed and conventional methods.

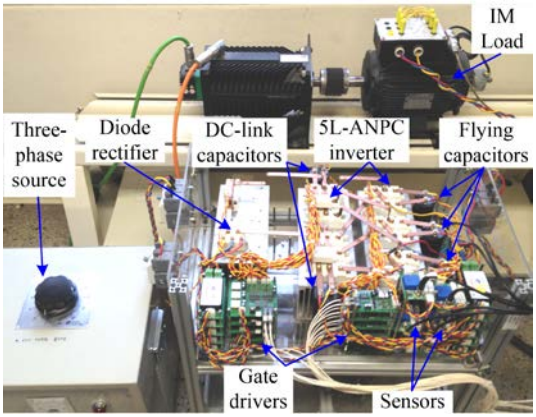

Fig. 16. Experimental setup of 5L-ANPC inverter.

TABLE IV. EXPERIMENTAL PARAMETERS OF 5L-ANPC INVERTERS

Parameters	Values
DC input voltage	320 V
DC-link capacitance	2,200 μF
Flying capacitance	1,000 μF
Switching frequency	2,000 Hz
Output voltage frequency	60 Hz
$\Delta v_{n\ max}$	8.0 V
$\Delta v_{f\ max}$	2.0 V

SVPWM of case-1, there are no redundant voltage vectors that can control the DC-link capacitor voltages, which is different from the regular SVPWM [20]. Instead, the redundant switching states are utilized, which can control selectively the DC-link and flying capacitor voltages. So, the fluctuation in the capacitor voltages is a little higher than that of in the conventional SVPWM. However, it is still within the allowable range.

The power losses of the 5L-ANPC inverter have been estimated from thermal model in PSIM software, where the devices of FZ250R65KE3 and FF200R33KF2C of Infineon manufacture have been employed. Fig. 15 show the power loss comparison of the conventional and proposed SVPWM methods at full load condition with 0.85 lagging power factor,

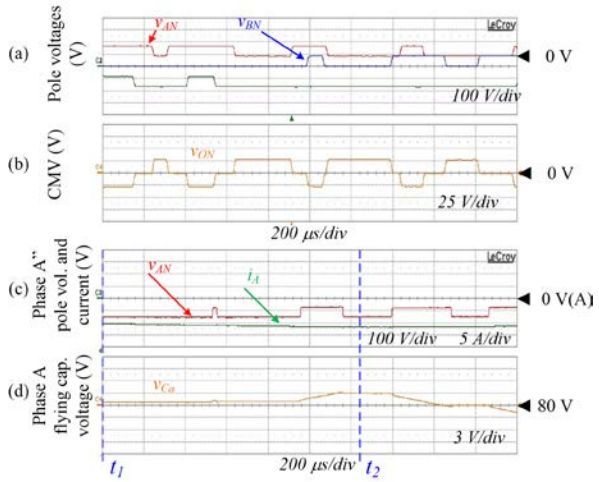

Fig. 17. Operating principle of the proposed method (experimental). (a) Three-phase pole voltages. (b) CMV. (c) Pole voltage and load current in phase-A. (d) Flying capacitor voltage in phase-A.

where P_con_pro and P_sw_pro represent the conduction and switching losses of the conventional method, respectively and P_con_cnv and P_sw_cnv means those of the proposed method, respectively. For the proposed SVPWM with the 55 available voltage vectors as shown in Fig. 4, a transition from a voltage vector to other nearest voltage vector requires only one change of the switching state in a leg. So, the changes of the switching state are not increased, resulting in no additional switching losses. On the contrary, in the conventional method, the flying capacitor voltage is controlled every sampling period, so that additional changes of the switching states between V_1 and V_2 or V_5 and V_6 exist, resulting in additional switching losses.

VI. EXPERIMENTAL RESULTS

The experimental set-up of 5L-ANPC inverter has been developed for testing of the proposed scheme at laboratory, of which photo is shown in Fig. 16. The system parameters of hardware are listed in Table IV. The IGBTs, SKM75GB12T4, of the inverter are controlled by a DSP chip of TMS320F28335 including 18 PWM gating signals, which were implemented by the Xilinx FPGA device (XC3S400-PQG208EGQ1321). The induction machine of 3 kW-220 V is driven by V/f method as the load to verify the proposed scheme. The switching frequency of the 5L-ANPC inverter is 2 kHz.

Fig. 17(a) and (b) show the three-phase pole voltages and the CMV, respectively. The CMV varying among the three voltage levels of $-V_{dc}/12$, 0, and $V_{dc}/12$ depends on the value of the pole voltages. The pole voltage and current in phase-A are shown in Fig. 17(c), by which the flying-capacitor voltage in phase-A varies as shown in Fig. 17(d). It is seen that the change of the flying-capacitor voltage occurs at the pole voltage level of $-V_{dc}/4$ to follow the reference value of $V_{dc}/4$. At t = t_1, the flying capacitor voltage is slightly higher

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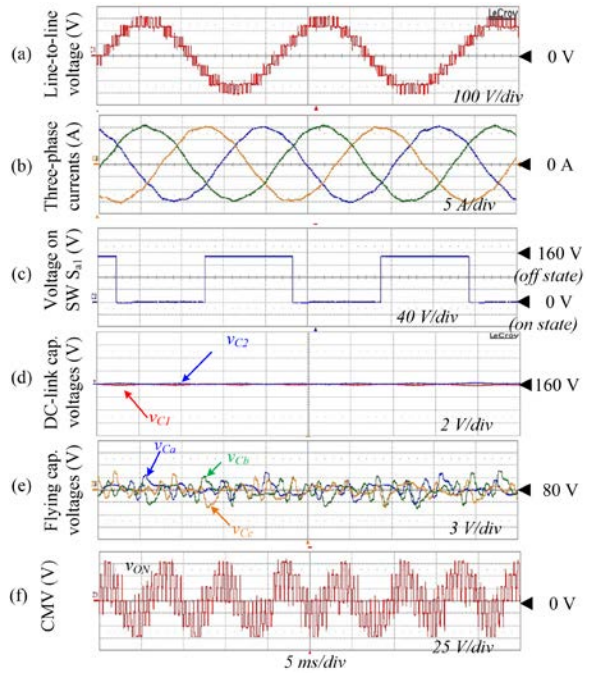

Fig. 18. Operation of the 5L-ANPC inverter with conventional scheme. (a) Line-to-line voltage. (b) Three-phase currents. (c) Gating signal of S_{a1}. (d) DC-link capacitor voltages. (e) Flying capacitor voltages. (f) CMV.

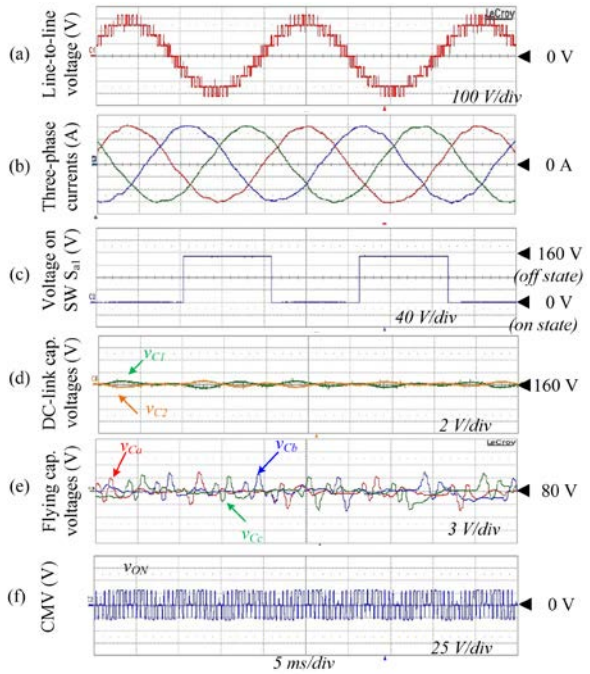

Fig. 19. Operation of the 5L-ANPC inverter with proposed scheme. (a) Line-to-line voltage. (b) Three-phase currents. (c) Gating signal of S_{a1}. (d) DC-link capacitor voltages. (e) Flying capacitor voltages. (f) CMV.

than the reference value and the flying capacitor is charged by the V_1 since the Sig_DC_a is utilized to control the DC-link capacitor voltage. Then, at time t = t_2, the flying capacitor voltage is higher than the Δv_{f_max}, the switching state of V_2 is applied to control the flying capacitors.

Fig. 18 shows the performance of the 5L-ANPC inverter with the conventional PWM method, which feeds the induction machine at rated speed. Fig. 18(a) shows the output voltage of the inverter with nine voltage levels. The three-phase currents are shown in Fig. 18(b), which are sinusoidal. The voltage applied to the switch S_{A1} is shown in Fig. 18(c), which implies that higher-rated voltage device is operated at the fundamental frequency. The DC-link capacitor voltages are balanced around their reference value of 160 V with a very low fluctuation of about 0.5 V as shown in Fig. 18(d). The three phase capacitor voltages of the inverter are shown in Fig. 18(e), with the peak of fluctuation around 4 V. The CMV of the inverter with the conventional method as illustrated in Fig. 18(f) varies from –80 V to 80 V with the RMS value of 43.5 V. For experiment, the waveform of the CMV with the conventional method is different from that of the simulation due to the different offset voltage for the DC-link capacitor voltage balancing.

Besides, the output performance of the inverter with the proposed scheme is shown in Fig. 19, in which the test conditions are the same as those of in Fig. 18. The THD of the output voltage in Fig. 19(a) is 16.8%, which is slightly higher than that of in the conventional method. Fig. 19(b) shows the three phase currents, which are almost sinusoidal. The proposed method keeps the higher-rated voltage switches operating at fundamental switching frequency as shown in Fig. 19(c), where the voltage in the switches is changed at fundamental frequency. The DC-link capacitor and flying capacitor voltages are controlled at the reference values of $V_{dc}/2$ and $V_{dc}/4$ with the error of 1 V and 4.5 V as shown in

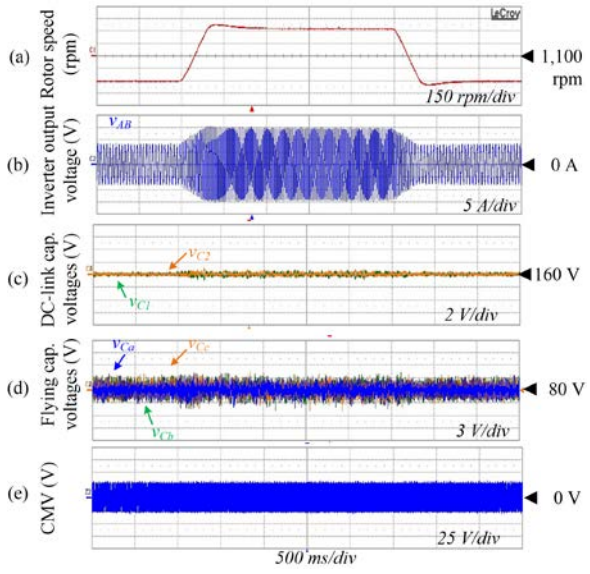

Fig. 20. Performance for motor speed variations. (a) Rotor speed. (b) Output voltage. (c) DC-link capacitor voltages. (d) Flying capacitor voltages. (e) CMV.

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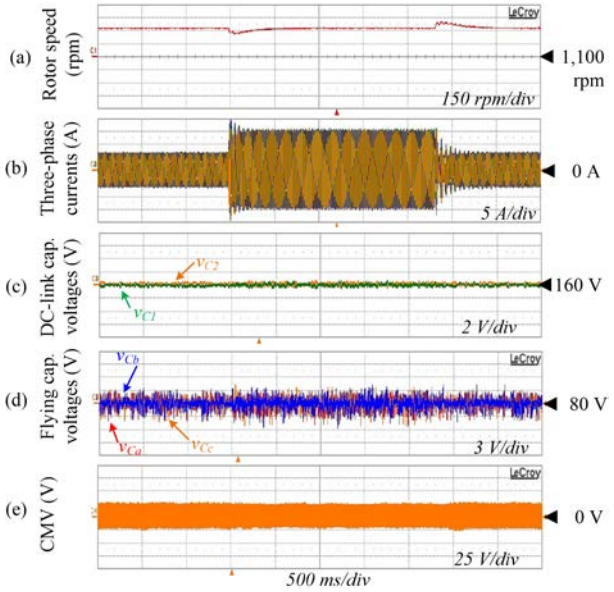

Fig. 21. Performance for load variations. (a) Rotor speed. (b) Motor current. (c) DC-link capacitor voltages. (d) Flying capacitor voltages. (e) CMV

Fig. 19(d) and (f), respectively. Fig. 19(f) shows the CMV of the inverter with the proposed SVPWM, in which the peak and RMS values are 26.7 V and 21.3 V, respectively. It is noted that the peak values of fluctuation in the flying-capacitor and DC-link capacitor voltages are slightly higher than those of the conventional PWM method. However, the peak and RMS values of the CMV are reduced significantly.

Fig. 20 show the performance of the inverter for motor speed variations, which is changed from 800 rpm to 1,430 rpm and back to 800 rpm as shown in Fig. 20(a). Although both the magnitude and frequency of the output voltage are changed, the DC-link and flying capacitor voltages are well controlled, which are shown in Fig. 20(c) and (d), respectively. The CMV is kept as $V_{dc}/12$, as shown in Fig. 20(e).

Fig. 21 shows the performance of the inverter for load variations, which is changed from no load to full load and back to no load condition. The capacitor voltages are well controlled as shown in Fig. 21(b) and (c), respectively. The CMV is also kept as $V_{dc}/12$, as shown in Fig. 21(d).

Fig. 22 shows the performance of the proto-type system, which corresponds to Fig. 13. The fluctuations of the DC-link and flying capacitor voltages are about 1% and 3.8%, respectively. Also, the CMV is reduced to $V_{dc}/12$ as in Fig. 22(f).

VII. Conclusion

This paper has proposed a novel SVPWM scheme to reduce the CMV of the 5L-ANPC inverter for medium-voltage and high-power induction motor drives, by which the CMV of the inverter is significantly reduced up to one

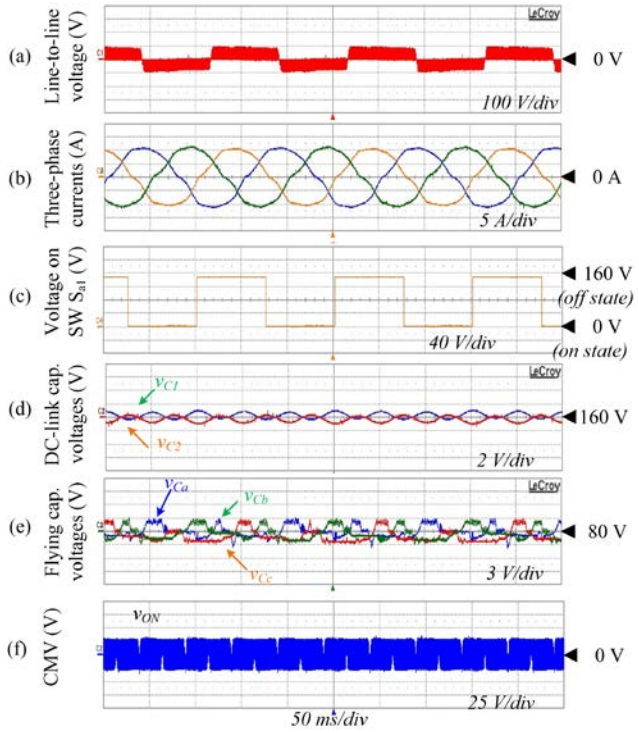

Fig. 22. Operation of the 5L-ANPC inverter at low speed of induction motor (experiment). (a) Line-to-line voltage. (b) Three-phase currents. (c) Gating signal of S_{a1}. (d) DC-link capacitor voltages. (e) Flying capacitor voltages. (f) CMV.

twelfth of the DC-link voltage. The peak and RMS values of the CMV in the proposed SVPWM method are about 33% and 78%, respectively, compared with those of in the conventional one. Even though only the 55 selected voltage vectors are utilized, both the DC-link and flying-capacitor voltages are well controlled by applying the redundant switching states appropriately. Furthermore, the switching losses are not increased as well as the utilization of the DC input voltage is not decreased. The performance of the proposed method is not deteriorated at low modulation index, which is also independent of power factor. The effective ness of the proposed method has been verified by the simulation and experimental results.

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